

## **CLAIMS**

### **WHAT IS CLAIMED IS:**

- 5     1. A method comprising:  
          detecting an event that would cause cycles to be idle in a processor; and  
          issuing diagnostic instructions to the processor during the cycles that would be  
          idle.
- 10    2. The method of claim 1, further comprising:  
          selecting the diagnostic instructions based on a number of the cycles that would  
          be idle.
- 15    3. The method of claim 1, further comprising:  
          comparing a result of the diagnostic instructions with a pre-computed result.
- 20    4. The method of claim 1, further comprising:  
          incrementing a pre-computed result between the diagnostic instructions wherein  
          the pre-computed result of one of the diagnostic instructions is input to a next of the  
          diagnostic instructions.
- 25    5. The method of claim 1, wherein the event comprises a cache miss.
6. The method of claim 1, wherein the event comprises a task switch.
7. An apparatus comprising:  
          means for detecting an event that would cause cycles to be idle in a processor;  
          means for issuing diagnostic instructions to the processor during the cycles that  
          would be idle; and

means for comparing a result of the diagnostic instructions with a pre-computed result.

8. The apparatus of claim 7, further comprising:

5 means for selecting the diagnostic instructions based on a number of the cycles that would be idle.

9. The apparatus of claim 7, further comprising:

10 means for incrementing a pre-computed result between the diagnostic instructions wherein the pre-computed result of one of the diagnostic instructions is input to a next of the diagnostic instructions.

10. A processor comprising:

15 an issue unit to detect an event that would cause cycles to be idle in the processor and issue diagnostic instructions during the cycles that would be idle to a pipeline;

an increment unit to increment a pre-computed result between the diagnostic instructions wherein the pre-computed result of one of the diagnostic instructions is input to a next of the diagnostic instructions; and

20 a compare unit to compare the pre-computed result with a result of each of the diagnostic instructions.

11. The processor of claim 10, wherein the issue unit is further to select the diagnostic instructions based on a number of the cycles.

25 12. The processor of claim 10, wherein the event comprises a cache miss.

13. The processor of claim 10, wherein the event comprises a task switch.

14. A computer system comprising:

a processor comprising a counter, wherein when the counter exceeds a threshold, diagnostic code is invoked;

a storage device encoded with the diagnostic code, wherein the diagnostic code when executed on the processor comprises:

5           selecting a test routine to issue to the processor based on an error log.

15. The computer system of claim 14, wherein the selecting further comprises:

          selecting the test routine to issue to the processor based on a history of activity at the processor.

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16. The computer system of claim 14, wherein the selecting further comprises:

          selecting the test routine to issue to the processor based on a temperature of a unit of the processor.

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17. The computer system of claim 14, wherein the diagnostic code further comprises:

          changing an interval of a count of activity at the processor based on activity of a unit of the processor and a temperature of a unit of the processor.

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18. A signal-bearing medium encoded with instructions, wherein the instructions when

executed comprise:

          periodically selecting a test routine to issue to a processor based on a log of errors at the processor and a history of activity at the processor.

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19. The signal-bearing medium of claim 18, wherein the periodically selecting further

comprises:

          selecting the test routine to issue to the processor based on a temperature of a unit of the processor.

20. The signal-bearing medium of claim 18, further comprising:

changing an interval of a count of activity at the processor based on activity of a unit of the processor and a temperature of a unit of the processor.